



United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

DATE MAILED: 04/04/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/039,650	12/31/2001	Shiv Kaushik	042390.P13636	9232		
. 7	590 04/04/2005	EXAM	EXAMINER			
Jeffrey S. Draeger BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP			HUISMAN	HUISMAN, DAVID J		
Seventh Floor			ART UNIT	PAPER NUMBER		
12400 Wilshire Boulevard			2183			

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.		Applicant(s)				
Office Action Summary								
		10/039,650 Examiner		KAUSHIK ET AL. Art Unit				
	,			2183				
The MAILING DATE	of this communication app	Charles A Harkne			Idraca			
Period for Reply	or this communication app	oears on the cover	Sheet with the C	orrespondence ad	aress			
 Failure to reply within the set or extended 	HIS COMMUNICATION. under the provisions of 37 CFR 1.1 ling date of this communication. e is less than thirty (30) days, a repl ove, the maximum statutory period v ended period for reply will, by statute er than three months after the mailing	36(a). In no event, howe by within the statutory min will apply and will expire to cause the application to	over, may a reply be tim imum of thirty (30) days SIX (6) MONTHS from b become ABANDONE	nely filed s will be considered timel the mailing date of this co O (35 U.S.C. § 133)				
Status								
1) Responsive to comm	unication(s) filed on 06 Ja	anuarv 2005.						
2a)⊠ This action is FINAL								
· <u>—</u>								
•	with the practice under E	•	•					
Disposition of Claims								
<u> </u>	122 io/aro pondina in the	application						
, , , , , , , , , , , , , , , , , , , ,	Claim(s) 1-23,31 and 32 is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
)[☐ Claim(s) is/are allowed.)[☑ Claim(s) <u>1-23 and 31-32</u> is/are rejected.							
	Claim(s) is/are objected to. Claim(s) are subject to restriction and/or election requirement.							
	asjour to roundian andro	·			•			
Application Papers								
9) The specification is objected to by the Examiner.								
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority under 35 U.S.C. § 119)							
2. Certified copie3. Copies of the capplication from		s have been rece s have been rece nty documents ha u (PCT Rule 17.2	ived. ived in Application ive been receiver (a)).	on No ed in this National	Stage			
Attachment(s)								
1) Notice of References Cited (PTC			Interview Summary					
 Notice of Draftsperson's Patent Information Disclosure Stateme Paper No(s)/Mail Date 02/18/05 	nt(s) (PTO-1449 or PTO/SB/08)	5) 🔲	Paper No(s)/Mail Da Notice of Informal P Other:	ate atent Application (PTC	D-152)			

Application/Control Number: 10/039,650

Art Unit: 2183

DETAILED ACTION

Page 2

1. In view of the amendment made to the title, the objection to the specification was been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 2. Claims 1-23 and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Emer et al., U.S. Patent Number 6,493,741 (herein referred to as Emer).
- 3. Referring to claims 1, 12 and 18 Emer has taught an article comprising a machine readable medium storing instructions that, if executed by a machine, cause the machine to perform a plurality of operations comprising:

specifying a monitor address;

suspending a thread until a monitor break event occurs;

testing whether the monitor break event is a write to a first value for a first task indicated by the monitor address;

testing whether the monitor break event is a write to a second value for a second task indicated by the monitor address (Emer column 3 lines 36-41);

if the monitor break event is not a write to the first value or a write to the second value, then suspending the thread again (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50).

Application/Control Number: 10/039,650

Art Unit: 2183

4. Referring to claim 2 and 13 Emer has taught wherein suspending the thread again comprises returning to specifying the monitor address (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50).

Page 3

- 5. Referring to claims 3 and 14 Emer has taught wherein programming the monitor comprises executing a MONITOR instruction and wherein suspending the thread until the monitor break event occurs comprises executing an MWAIT instruction (Emer column 5 lines 28-40).
- 6. Referring to claims 4 and 15 Emer has taught wherein said plurality of operations further comprise, after programming the monitor address and before suspending the thread: testing whether the first value or the second value has changed (Emer figure 9 column 11 line 1-column 12 line 35).
- 7. Referring to claims 5 and 16 Emer has taught wherein specifying the monitor address comprises executing an instruction with an implicit operand specifying a linear address (Emer column 5 lines 28-40).
- 8. Referring to claims 6 and 17 Emer has taught wherein the operand is an implicit operand (Emer column 5 lines 28-40).
- 9. Referring to claim 7 Emer has taught wherein said monitor address specifies a cache line and wherein said first value and said second value are respectively stored in a first and second separate work location in the cache line (Emer figure 3 column 6 lines 12-30, column 7 lines 51-65).

Art Unit: 2183

- 10. Referring to claims 8 and 19 Emer has taught wherein said plurality of operations further comprise providing a second operand as a mask operand to control which events are monitor break events (Emer column 11 line 38-column 12 line 6, table in column 9).
- 11. Referring to claim 9 Emer has taught an article comprising a machine readable medium storing instructions that, if executed by a machine, cause the machine to perform operations comprising:

programming a monitor with a monitor address corresponding to a cache line of at least one work location (Emer column 5 lines 28-40; figure 3 column 6 lines 12-30, column 7 lines 51-65);

suspending a thread until a monitor break event occurs (Emer figure 8, column 3 lines 28-67, column 14 lines 27-50);

testing whether the at least one work location indicates a first task is ready to execute (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67);

testing whether the at least one work location indicates a second task is ready to execute (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67);

if neither the first task nor the second task is ready to execute, then returning to suspending the thread (Emer figure 3 figure 8, column 3 lines 28-67, column 14 lines 27-50, column 5 line 51-column 6 line 67).

12. Referring to claim 10 Emer has taught wherein returning to suspending the thread until the monitor break event occurs further comprises re-programming the monitor with the monitor

address prior to suspending the thread (Emer figure 9 column 11 line 1-column 12 line 35, column 5 lines 28-40).

Page 5

- 13. Referring to claim 11 Emer has taught wherein returning to suspending the thread comprises returning to programming the monitor with the monitor address (Emer figure 9 column 11 line 1-column 12 line 35, column 5 lines 28-40).
- 14. Referring to claim 20 Emer has taught a system comprising: a processor,

a monitor to generate a monitor break event in response to a memory access to a monitor address (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50);

event detect logic to detect an of a plurality of monitor break events; a memory to store a loop in a first thread executable by said processor to specify said monitor address and to repeatedly suspend said first thread after monitor break events until the memory access to the monitor address occurs (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50), the loop comprising:

a test to determine whether a work location in a first cache line indicated by the monitor address contains a first value wherein a first routine is executed if said work location contains the first value (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50);

a second test to determine whether the work location in said first cache line contains a second values wherein a second routine is executed if said work location contains the second value (Emer column 3 lines 36-41),

an instruction to suspend said first thread if said work location does not contain said first value and said work location does not contain said second value (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50).

Application/Control Number: 10/039,650 Page 6

Art Unit: 2183

15. Referring to claim 21 Emer has taught wherein said loop comprises:

a first instruction to specify the monitor address; a second instruction to suspend said first thread (Emer column 5 lines 28-40).

- 16. Referring to claim 22 Emer has taught wherein said loop further comprises a test after said first instruction to determine whether data at the monitor address has changed after execution of the first instruction but before execution of the second instruction, wherein said loop exits without execution of the second instruction if data at the monitor address has changed (Emer figure 9 column 11 line 1-column 12 line 35).
- 17. Referring to claim 23 Emer has taught wherein said loop further comprises a test after said first instruction to determine whether data at the monitor address has changed after execution of the second instruction wherein said loop performs another iteration if data at the monitor address has not changed (Emer figure 2 figure 8, column 3 lines 28-67, column 14 lines 27-50).
- 18. Referring to claim 31 Emer has taught where said monitor is programmable by a monitor instruction having an implicit operand (Emer column 5 lines 28-40; figure 3 column 6 lines 12-30, column 7 lines 51-65).
- 19. Referring to claim 32 Emer has taught wherein said implicit operand is to specify a linear address (Emer column 5 lines 28-40; figure 3 column 6 lines 12-30, column 7 lines 51-65).

Response to Arguments

20. Applicant's arguments filed 01/06/05 have been fully considered but they are not persuasive.

Art Unit: 2183

21.

In the remarks, in regard to the rejection of the claims, Applicant argues in essence that:

"Emer does not detail a situation in which multiple variables (e.g., lock variables) may be

stored in a memory region monitored by monitor software."

22. This is not found persuasive. Emer has taught having multiple processors, each having an

event timer, therefore having multiple events being monitored by software.

23. Emer has taught using the "spin lock" in a wait loop to be used as the event locking

protocol where an event is monitored and the event value must change before the process can

continue (Emer Column 2 lines 28-34). And in addition, Emer has taught that an event may be,

for example, a modification to some identified memory location or group of locations, such as a

change of access state or a change of value stored in the location. A change of access state may

be, for example, from shared to exclusive. Such an event is typically caused by another

program (Emer column 3 lines 36-41). Therefore, Emer is having multiple addresses checked

by the system, or multiple values checked by the system, in memory, and is being monitored by

software.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

Application/Control Number: 10/039,650

Art Unit: 2183

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579 and 571-272-4167 after 10/12/04. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

March 24, 2005

Page 8